WEST Search History

DATE: Thursday, August 21, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L4	(frequenc$3 near3 range$ near3 (select$3 or choos$3 or detect$3)) and (wideband near2 pll or (wideband near3 (phase adj lock$3 adj loop)))	3	L4
L3	(frequenc$3 near3 range$ near3 (select$3 or choos$3 or detect$3)) and (wideband near2 pll or (wideband near3 (phase adj lock$3 adj loop))) and (input near frequenc$3 near4 (detect$3 or measur$3))	0	L3
L2	(frequenc$3 near3 range$ near3 (select$3 or choos$3 or detect$3)) and (pll or (phase adj lock$3 adj loop)) and (input near frequenc$3 near4 (detect$3 or measur$3))	52	L2
L1	(frequenc$3 near3 range$ near3 (select$3 or choos$3 or detect$3)) same (pll or (phase adj lock$3 adj loop)) same (input near frequenc$3 near4 (detect$3 or measur$3))	0	L1

END OF SEARCH HISTORY

WEST Search History

DATE: Thursday, August 21, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT;JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1 and (375/$3.ccls.)	22	L2
L1	(frequency near3 range$ near3 (select$3 or choos$4)) same (pll or (phase adj2 lock$3 adj loop$))	158	L1

END OF SEARCH HISTORY

L2: Entry 2 of 22 File: USPT Mar 19, 2002

DOCUMENT-IDENTIFIER: US 6359983 B1
TITLE: Digital isolation system with data scrambling

Detailed Description Text (69):
In the presently preferred embodiment, a low-power mode is implemented by allowing the master oscillator, such as 704 in FIG. 7, to free-run when powered circuitry on the master side of the barrier is shut down to save power. Referring to FIG. 17, in normal operation, the local clock circuit, which may be a phase-locked-loop (PLL) circuit 334 including a voltage controlled oscillator (VCO) 336, locks to a timing signal CLK received from other circuitry 338 on the powered side of the telephone equipment. (Specifically, VCO 336 normally receives an input voltage from a loop filter in the PLL circuit 334, as is well known in the art.) When powered system 338 is placed in low power mode to conserve power, the timing signal CLK may be lost. In order to maintain a signal across barrier 209, 210 to the isolated circuitry 226 in such a case, the VCO input may be disconnected from the loop filter and connected to a constant bias voltage generator 340. VCO 336 then continues to oscillate in a selected frequency range based on the bias voltage, thus providing a local clock signal LCLK even when powered system 338 stops providing clock signal CLK. In a preferred embodiment, powered system 338 provides a low power mode signal LPM to isolation system 330 to communicate that it is about to enter low power mode, so that isolation system 330 can prepare to change modes of operation.

Current US Cross Reference Classification (1):
375/285

L2: Entry 6 of 22 File: USPT Oct 5, 1999

DOCUMENT-IDENTIFIER: US 5963608 A
TITLE: Clock extractor for high speed, variable data rate communication system

Brief Summary Text (9):
The data rate estimate code output by variable bit rate estimator 11 is coupled to a direct digital synthesizer and range selector controller 17, which operates on a first parsed segment (comprising a plurality of most significant bits) of the bit rate estimate code to set the output of a very precise numerically controlled oscillator within a direct digital synthesizer (DDS) 19. A divide-by-N divisor is used to define the divisor value of an octave divider within an `inner` phase locked loop (PLL) 21, through which a scaled-up frequency derived from the precision reference clock signal generated by DDS 19 is scaled into a selected range of frequencies for deriving a variable bit sync clock signal, that is applied to a digital phase detector 25. A second parsed segment (a group of least significant bits) of the bit rate estimate code is used by the controller 17 to generate a multi-bit DDS control word (and associated write control signals) representative of the frequency to be generated by a very precise numerically controlled oscillator within the DDS 19.

Current US Original Classification (1):
375/373

Current US Cross Reference Classification (1):
375/327

L2: Entry 8 of 22 File: USPT Nov 17, 1998

DOCUMENT-IDENTIFIER: US 5838749 A
TITLE: Method and apparatus for extracting an embedded clock from a digital data signal

Detailed Description Text (20):
This first precision reference clock signal is applied to a first, tunable `inner` phase locked loop. Based upon the bit frequency estimate derived by the bit rate estimator, the output of the first phase locked loop is scaled to a frequency range (octave) selected in accordance with the bit frequency estimate, so that the first tunable phase lock loop produces data rate clock signal VBSCLOCK that falls within that range. This VBSCLOCK signal is coupled to the descrambler 76 and the decoder 77.

Detailed Description Text (25):
The multi-bit data rate estimate code output by variable bit rate estimator 81 is coupled via a multi-bit link 91 to a direct digital synthesizer (DDS) and range selector controller 83, shown in detail in FIG. 12, to be described. DDS and range selector controller 83 operates on a first parsed segment (comprising a plurality of most significant bits) of the bit rate estimate code to select an N divisor value employed by a first, .times.128/N phase locked loop circuit 85 (described in detail below with reference to FIG. 14). This divide-by-N divisor is used to define the divisor value of an octave divider within phase locked loop circuit 85, through which a scaled-up frequency derived from a precision reference clock signal (2.34375 to 4.68750 MHz) generated by a direct digital synthesizer 87 is scaled down or subdivided into a selected range of frequencies for deriving a variable bit sync clock signal, which is applied to a digital phase detector 84 (shown in detail in FIG. 15, to be described). A second parsed segment (formed of a group of least significant bits) of the bit rate estimate code is used by the DDS and range selector controller 83 to generate a thirty-two bit DDS control word (and associated write control signals) representative of the frequency to be generated by a very precise numerically controlled oscillator within the DDS 87.

Current US Original Classification (1):
375/376